Chrysostomos Nicopoulos, Ph.D.

Curriculum Vitae

26 April 2018

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Chrysostomos Nicopoulos, Ph.D.

Department of Electrical and Computer Engineering (ECE)
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Education

- *August 2007 (Official Degree Conferral: December 2007)*
  Ph.D. in Electrical Engineering (Specialization in **Computer Engineering**)
  - The Pennsylvania State University, University Park, PA 16802, USA
  - Thesis Title: "**Network-on-Chip Architectures: A Holistic Design Exploration**"
    - Ph.D. Thesis received the **2008 Outstanding Dissertation Award** in the area of "New directions in logic and system design" by the European Design and Automation Association (EDAA)
  - Thesis Adviser: Prof. Vijaykrishnan Narayanan
  - GPA: 3.94/4.00

- *May 2003*
  B.Sc. in Electrical Engineering with Minor in Mathematics
  - The Pennsylvania State University, University Park, PA 16802, USA
  - Graduated from **Schreyer Honors College** (Penn State Honors Program)
    - Honors Thesis Title: "Smart Antennas for Wireless Communications"
  - GPA: 4.00/4.00 (**Rank: 1/335**)

Research Interests

Founder and current leader of the **Multicore Computer Architecture Laboratory (multiCAL)** (http://multical.ece.ucy.ac.cy), conducting research in the areas of:

- Network-on-Chip (NoC) Architectures / On-Chip Interconnection Networks
- Computer Architecture
- Reliable and Fault-Tolerant Computer Architecture
- Microprocessor & Computer System Design
- Digital System Design

Teaching Interests

- *General Topics (Undergraduate-level)*
  - Computer Organization & Microprocessors
  - Computer Architecture
  - Digital Logic Design
  - VLSI Digital System Design
- *Advanced Topics (Graduate-level)*
  - Network-on-Chip (NoC) Architectures
  - Fault-Tolerant Computer Architecture
  - Chip Multi-Processors (CMP) / Multi-Processor Systems-on-Chip (MPSoC)
  - Cache/Memory Hierarchy
  - Architectural Ramifications of Emerging Memory Technologies
  - Performance/Area/Power/Reliability/Variability Tradeoffs in Digital System Design
  - Full-System Simulation / FPGA Prototyping

Employment

- *April 2018 – Present*

  Associate Professor (tenured), Department of Electrical and Computer Engineering (ECE), University of Cyprus

- *January 2013 – March 2018*

  Assistant Professor, Department of Electrical and Computer Engineering (ECE), University of Cyprus
  - Taught various courses in electrical and computer engineering, performed scholarly research, and supervised undergraduate/graduate students with their academic projects and Bachelor's, Master's, and Ph.D. theses.
  - Fostered numerous national and international research collaborations with other research groups.

- *January 2009 – December 2012*

  Lecturer, Department of Electrical and Computer Engineering (ECE), University of Cyprus
  - Taught various courses in electrical and computer engineering, performed scholarly research, and supervised undergraduate/graduate students with their academic projects and Bachelor's, Master's, and Ph.D. theses.
  - Established a research laboratory in the area of Computer Architecture.

- *September 2007 – June 2008*

  Postdoctoral Research Associate, I&C School of Computer and Communication Sciences, Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland
  - Member of the *Processor Architecture Laboratory*.
  - Research in the areas of Computer Architecture (specifically, Non-Uniform Cache Architectures), FPGAs, Field Programmable Counter Arrays (FPCA), Computer Arithmetic, Analytical Models of Communication for MPSoCs, and 3D System Architectures.

Honors & Awards

- **Ph.D. Thesis Award**
  - Recipient of the very prestigious European Design and Automation Association (EDAA) 2008-09 **Outstanding Dissertation Award for Ph.D. Thesis**. This award is presented annually to the **best Ph.D. thesis in the world** in the area of "New directions in logic and system design."
- **Best-Paper Awards**
  - **IEEE Best Paper Award** (with A. Psarras, I. Seitanidis, and G. Dimitrakopoulos), at the *IEEE/ACM Design Automation and Test in Europe (DATE) Conference*, March 2015 (Europe's premiere and biggest electronic system design & test conference; competitive, with an acceptance rate of 22.4% for long/short presentations in that particular year).
  - **HiPEAC 2012 Paper Award** (with A. Prodromou, A. Panteli, and Y. Sazeides), for paper presented at the 45^{th} *Annual International Symposium on Microarchitecture (MICRO)*, December 2012 (annual award by the HiPEAC European Network of Excellence).
  - **IEEE Best Paper Award** (with S.C. Kang, H. Lee, and J. Kim), at the *IEEE International Conference on High Performance Computing and Communications (HPCC)*, September 2011.
- **Best-Paper Award Nominations**
  - **IEEE Best Paper Award Nomination** (with I. Seitanidis and G. Dimitrakopoulos), at the *IEEE Symposium on Networks-on-Chip (NOCS)*, September 2016. (Main annual conference in the area of Networks-on-Chip (NoC)).
  - **IEEE Best Paper Award Nomination** (with J. Lee, Y. Lee, H. Lee, and J. Kim), at the *IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, May 2011 (Competitive conference with an acceptance rate of 19.6% in that particular year).
- **Awards won by Supervised Students**

- Panayiotis Englezakis, **University of Cyprus Ph.D. Scholarship** – Scholarship includes annual stipend and tuition fee waiver, September 2017 – September 2018.
- Solon Falas, **Best Senior Design Project** in Computer Engineering, 2017.
- Georgios Klokkaris, **Best Senior Design Project** in Computer Engineering, 2012.
- Andreas Panteli, **Best Senior Design Project** in Computer Engineering, 2011 (shared with A. Prodromou; see below).
- Andreas Prodromou, **Best Senior Design Project** in Computer Engineering, 2011 (shared with A. Panteli; see above).

- **Other Awards**
  - Recipient of the Evan Pugh Scholar Award at Penn State in April 2003 (**Upper 0.5 percent of graduating class**)
  - Recipient of a College of Engineering **Graduate Fellowship** at Penn State in March 2003
  - Recipient of a 3-year **Graduate Fellowship** from the Electrical Engineering Department at Penn State in March 2003
  - Awarded a **Fulbright Scholarship** to study in the USA in 1998
  - Selected to represent Cyprus in the World Debating and Public Speaking Championships in 1995
  - Selected as member of the Cyprus Delegation in the European Youth Parliament's 1995 session in Gothenburg, Sweden
  - **Pan-Cyprian Champion** in the Toastmasters Public Speaking Competitions (in both Greek and English competitions) in 1994

Teaching Activities

Teaching Evaluation Statistics:

The following statistics are derived from the grades recorded in the **Course Evaluation Forms** that all students complete at the end of each course.

Since joining the University of Cyprus in January 2009, C. Nicopoulos has received consistently high teaching evaluation grades:

- Lowest Average Course Grade: 3.83 / 5.00
- Highest Average Course Grade: 5.00 / 5.00
- **Average Course Grade** across all taught courses: **4.55 / 5.00** (**91%**)

All *Course Evaluation Summaries* are available upon request.

Courses Taught (The * symbol denotes newly developed course)

[2XX/3XX/4XX – Undergraduate, 6XX/7XX – Graduate]

- ECE 212 – Computer Organization & Microprocessors (Spring 2010 – Spring 2018)
  Introductory course in modern computer organization and architecture. Topics include: machine language, instruction set architecture (MIPS), computer arithmetic, performance analysis and improvement, microprocessor design, datapath and control unit design, pipelining, and memory hierarchy.
- ECE 314* – Computer Architecture Laboratory (Fall 2017)
  Junior-level course for computer engineering students to provide hands-on experience with basic design and evaluation concepts in computer architecture. Cycle-accurate simulation tools are used for modeling and evaluation. Laboratory exercises include design of processor datapath and control unit, memory hierarchy, pipelining, and branch predictors.
- ECE 317 – Software Engineering (Spring 2009)
  Software requirements and specifications, modeling, implementation strategies, testing, verification and validation, ethics, project management, teamwork skills.

- ECE 401/402 – Capstone Design Project I/II (Every academic year since Fall 2009)
  Full-year (Fall/Spring semesters) capstone design project for fourth-year (senior) electrical and computer engineering students. Each faculty member supervises a few students per academic year. Supervisor sets the project topic and detailed specifications/requirements for each of the supervised students. Course involves weekly face-to-face meetings with each supervised student, until the successful completion and final evaluation of the project.
- ECE 409* – Computer Architecture II (Spring 2010, Fall 2010 – Fall 2016)
  Senior-level undergraduate course in computer architecture. Topics include the impact of technology on system design, superscalar architectures, register renaming, prediction, speculation, out-of-order execution, VLIW, dynamic binary translation, low power techniques, introduction to CMPs.
- ECE 656* – Advanced Computer Architecture (Fall 2009, Fall 2011 – Fall 2015, Fall 2017)
  Advanced ILP/superscalar design concepts, instruction supply/flow techniques, register data flow techniques (dynamic scheduling), memory data flow mechanisms, vector processors, Thread-Level Parallelism (TLP), multi-threading, multi-processors, message-passing and shared-memory programming models, memory consistency models, cache coherence protocols (snoop-/directory-based).
- ECE 798* – Network-on-Chip (NoC) Architectures (Fall 2016)
  Advanced concepts in on-chip interconnection networks. Topics include state-of-the-art micro-architectural techniques, such as speculative and combined allocation, router- and pipeline-bypassing mechanisms, low-power and high-performance optimizations, and fault-tolerant design principles. System-level interactions within the context of multi-/many-core microprocessors (e.g., cache-coherence assistance, application-level isolation, etc.) are also covered. Overview of latest developments in the field.
- ECE 701/704/705 – Graduate Seminar Series (M.Sc./M.Eng./Ph.D. students) (Spring 2011, Spring 2018)
  Seminar lectures for all graduate students (i.e., M.Sc., M.Eng., and Ph.D.) in various topics of Electrical and Computer Engineering. Course coordination includes speaker invitation, scheduling, and chairing of seminar lectures.
- ECE 711 – Independent Study (M.Sc./M.Eng./Ph.D. students) (Spring 2009, Fall 2010, Fall 2011)
  Individual study at the graduate level of special topics not covered, or not regularly offered, by the department. Topics covered include the design and implementation of high-performance, low-power, and fault-tolerant Network-on-Chip (NoC) architectures. Advanced concepts and principles in NoC design were also covered.

Academic Advising

- **Current Students**
  - Panayiotis Englezakis, Ph.D. Student (expected graduation: June 2020; **candidate level**)
    Research Area: Fault-tolerant NoC architectures
- **Graduated Students at UCY**
  - Michalis Skitsas, Ph.D. [co-advised with Dr. M. Michael], December 2017 **(Currently Software Engineer and Research Scientist at ADITESS Ltd., Cyprus)**
    Thesis Title: "O/S-enabled on-line Software-Based Self-Test and Recovery for Resilient Shared-Memory Multicore Systems"
  - Kypros Chrysanthou, M.Sc., June 2017 **(Currently Software Developer at Amdocks Development Ltd., Cyprus)**
    Thesis Title: "A Fault Localization Mechanism for Network-on-Chip Architectures"
    Part of his work was published in **ACM TACO (2016)** and **IEEE TVLSI (2015)**
  - Georgios Klokkaris, M.Sc., December 2014 **(Currently Engineer at ARM Holdings plc, UK)**
    Thesis Title: "Offline and Online Estimation of Performance Degradation Due to Aging Faults in Caches"
  - Nikodemos Georgiades, M.Sc., July 2014 **(Currently Software Developer at Fourth GL Prodata Ltd., Cyprus)**

Thesis Title: "SNoC: A Snoop-Based NoC Design for Unordered Interconnects"
Part of his work was published at **DATE-2013**

– Andreas Panteli, M.Sc., May 2013 **(Currently I.T. Engineer at The Cyprus Institute, Cyprus)**
Thesis Title: "NoCAlert: Protecting the Network-on-Chip with an On-Line and Real-Time Checking Mechanism"
Part of his work was published at **MICRO-2012**

– Andreas Prodromou, M.Sc., May 2013 **(Currently a Ph.D. student at UCSD, USA)**
Thesis Title: "Detection and Localization of Faults in Network-on-Chip Routers via Invariance Checking"
Part of his work was published at **MICRO-2012**

– Marios Evripidou, M.Sc., December 2011 **(Currently Software Developer at Point Nine Ltd., Cyprus)**
Thesis Title: "Virtualizing Virtual Channels for Increased Network-on-Chip Robustness and Reliability"
Part of his work was published at **ISVLSI-2012**

- **Graduated Students at Other Universities**
  - Actively engaged in guiding the Ph.D. studies of Anastasios Psarras at the **Democritus University of Thrace, Greece** (graduated in June 2017). Co-authored all papers pertaining to his Ph.D. work (see list of publications), and served on his Ph.D. evaluation committee.
  - Actively engaged in guiding the Ph.D. studies of Junghee Lee and Seungcheol Baek at the **Georgia Institute of Technology, USA** (graduated in 2013 and 2014, respectively). Co-authored all papers pertaining to their Ph.D. work (see list of publications).

- **M.Sc./Ph.D. Committees**
  - Ph.D. Thesis Defense Committees: 7 Ph.D. candidates (5 at UCY, 1 at the Cyprus University of Technology, Limassol, Cyprus, and 1 at Democritus University of Thrace, Greece)
  - Ph.D. Thesis Proposal Committees: 4 Ph.D. candidates
  - M.Sc. Thesis Committees: 14 M.Sc. candidates (9 in ECE Department and 5 in CS Department)
  - Ph.D. Qualifying Examination Committees: 4 Ph.D. candidates

- **Undergraduate-level Advising**
  - Supervised (as sole advisor) the Capstone Design Projects of 15 senior-level undergraduate students since Fall 2009. Four of those students won the **Best Senior Design Project Award** in their respective year.
  - Served on the evaluation committees of several more Capstone Design Projects.

Grants, Funded Research Projects, and Research Contracts

- **External Research Funding**
  - *Intel Hardware Accelerator Research Program*, 12.2016 – 12.2019, Awarded by Intel Corporation, USA.
    - **Co-Principal Investigator** (with 4 other Co-PIs: T. Theocharides, M. Michael, Y. Sazeides, and P. Trancoso)
    - World-wide competitive program evaluated on technical merit, potential impact of the proposed research, and potential for collaboration with Intel researchers.
    - No *direct* monetary compensation. Granted access to Intel's computer clusters containing state-of-the-art heterogeneous microprocessor systems combining Intel Xeon CPUs and Altera FPGAs, and incorporating Intel's Accelerator Abstraction Layer Software. Furthermore, the program provides our researchers exclusive access to a series of workshops to be held at Intel campuses.

  - "Harnessing Performance Variability (HARPA)," 09.2013 – 12.2016, European Union 7th Framework Program (FP7) STREP.

    - University of Cyprus **Co-Principal Investigator** (other Co-PI: Yiannakis Sazeides, Department of Computer Science, University of Cyprus)
    - Amount: **EUR 3,889,643** (of which **EUR 506,488 to University of Cyprus**)
    - Consortium Partners: POLIMI (Italy), IMEC (Belgium), NTUA/ICCS (Greece), IT4Innovations (Czech Republic), THALES (France), HENESIS S.R.L. (Italy)

  - "Energy-Conscious 3D Server-on-Chip for Green Cloud Services (EuroCloud)," 01.2010 – 12.2012, European Union 7th Framework Program (FP7) STREP.
    - University of Cyprus **Co-Investigator** (Principal Investigator: Yiannakis Sazeides, Department of Computer Science, University of Cyprus)
    - Amount: **EUR 3,292,000** (of which **EUR 498,418 to University of Cyprus**)
    - Consortium Partners: Nokia Corp. (Finland), ARM Holdings (UK), EPFL (Switzerland), IMEC (Belgium)

  - "Mnemosyne: An Intelligent On-Chip Network for the Cache/Memory Sub-System of Chip Multi-Processors," 12.2010 – 12.2012, Cyprus Research Promotion Foundation.
    - **Principal Investigator**
    - Amount: **EUR 148,060** (of which **EUR 101,440 to University of Cyprus**)
    - Consortium Partners: Cyprus University of Technology, EPFL (Switzerland), IBM Italia SpA (Cyprus Branch)

- **Internal Research Funding**
  - "Multicore Computer Architecture Laboratory," 2010-11, University of Cyprus Internal Research Funds, Start-Up Funding.
    - **Principal Investigator**
    - Amount: **EUR 85,000**

- **External Formal Research Contracts**
  - "Exploration of Architectural Components Implementing Neuromorphic Computing Kernels," 01.2017 – 12.2020, Formal Research Contract with Interuniversitair Micro-Electronica Centrum (IMEC) VZW, Belgium, and Stichting IMEC Nederland.
    - University of Cyprus **Co-Principal Investigator** (other Co-PI: Yiannakis Sazeides, Department of Computer Science, University of Cyprus)
    - Amount: No *direct* monetary compensation, but the contract includes access to IMEC facilities and technical expertise, M.Sc./Ph.D. student internships at IMEC, and M.Sc./Ph.D. co-advising between IMEC and UCY.

Publications

Chrysostomos Nicopoulos

FOLLOW

Associate Professor, Department of ECE, University of Cyprus
Verified email at ucy.ac.cy - Homepage
Networks-on-Chip (NoC) Computer Architecture Microprocessor Design

Cited by		VIEW ALL
	All	Since 2013
Citations	2779	1480
h-index	20	19
i10-index	36	32

Citation statistics (as reported by *Google Scholar* on 26 April 2018):

Total **# of Citations: 2,779**
h-index: 20
i-10 index (# of publications with at least 10 citations): **36**
# of publications with **at least 100 citations: 6** (details below)
# of citations of top 6 publications: 448, 331, 279, 247, 247, 123 (see Google Scholar)

Books

[B1] C.A. Nicopoulos, N. Vijaykrishnan and C.R. Das, "Network-on-Chip Architectures: A Holistic Design Exploration," *Lecture Notes in Electrical Engineering Book Series*, Springer, October 2009. ISBN: 978-90-481-3030-6.

[Published by Springer as part of the European Design and Automation Association (EDAA) 2008-09 Outstanding Ph.D. Dissertation Award]

Book Chapters

[BC3] D. Zoni, P. Englezakis, K. Chrysanthou, A. Canidio, A. Prodromou, A. Panteli, C. Nicopoulos, G. Dimitrakopoulos, Y. Sazeides, and W. Fornaciari, "Monitor and Knob Techniques in Network-on-Chip Architectures," Chapter in *the book "Harnessing Performance Variability in Embedded and High-performance Many/Multi-core Platforms - A Cross-layer Approach,"* Springer, summer 2018.

[BC2] M.A. Skitsas, C. Nicopoulos, M.K. Michael, P. Bernardi, and E. Sanchez, "Self-testing of multi-core processors," Chapter 15 in *the book "Many Core Computing: Hardware and Software,"* Institution of Engineering and Technology (IET) Publishing, summer 2018.

[BC1] T. Theocharides, C.A. Nicopoulos, K. Irick, N. Vijaykrishnan, and M. J. Irwin, "An Exploration of Hardware Architectures for Face Detection," in the *VLSI Handbook*, Second Edition, CRC Press, Taylor & Francis Group, Chapter 83, 2007.

Journal Articles

[J27] I. Seitanidis, C. Nicopoulos, and G. Dimitrakopoulos, "Automatic Generation of Peak-Power Traffic for Networks-on-Chip," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, available online since February 2018, DOI: 10.1109/TCAD.2018.2801223.

[J26] M.A. Skitsas, C. Nicopoulos, and M.K. Michael, "Exploring System Availability during Software-Based Self-Testing of Multi-core CPUs," in *Springer Journal of Electronic Testing – Theory and Applications (JETTA)*, Volume 34, Issue 1, pp. 67-81, February 2018.

[J25] A. Psarras, S. Moisidis, C. Nicopoulos, and G. Dimitrakopoulos, "Networks-on-Chip with Double-Data-Rate Links," in *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Volume 64, Issue 12, pp. 3103-3114, December 2017.

[J24] A. Savva, T. Theocharides, and C. Nicopoulos, "A Design Space Exploration Framework for ANN-Based Fault Detection in Hardware Systems," in *Journal of Electrical and Computer Engineering*, Volume 2017, Article ID: 9361493, Digital Object Identifier (DOI): 10.1155/2017/9361493, December 2017.

[J23] A. Psarras, M. Paschou, C. Nicopoulos, and G. Dimitrakopoulos, "A Dual-Clock Multiple-Queue Shared Buffer," in *IEEE Transactions on Computers (TC)*, Volume 66, Issue 10, pp. 1809-1815, October 2017.

[J22] D. Zoni, A. Canidio, W. Fornaciari, P. Englezakis, C. Nicopoulos, and Y. Sazeides, "BlackOut: Enabling fine-grained power gating of buffers in Network-on-Chip routers," in *Elsevier Journal of Parallel and Distributed Computing (JPDC)*, Volume 104, pp. 130-145, June 2017.

[J21] J. Park, S. Baek, H.G. Lee, C. Nicopoulos, V. Young, J. Lee, and J. Kim, "HoPE: Hot-cacheline Prediction for Dynamic Early Decompression in Compressed LLCs," in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Volume 22, Issue 3, Article No. 40, April 2017.

[J20] A. Psarras, I. Seitanidis, C. Nicopoulos, and G. Dimitrakopoulos, "ShortPath: A Network-on-Chip Router with Fine-Grained Pipeline Bypassing," in *IEEE Transactions on Computers (TC)*, Volume 65, Issue 10, pp. 3136-3147, October 2016.

[J19] M. Alam, Z.C. Lee, C. Nicopoulos, K.H. Lee, J. Kim, and J. Lee, "SBBox: A Tamper-Resistant Digital Archiving System," in *International Journal of Cyber-Security and Digital Forensics (IJCSDF)*, Volume 5, Issue 3, pp. 122-131, August 2016.

[J18] K. Chrysanthou, P. Englezakis, A. Prodromou, A. Panteli, C. Nicopoulos, Y. Sazeides, and G. Dimitrakopoulos, "An Online and Real-Time Fault Detection and Localization Mechanism for Network-on-Chip Architectures," in *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 13, Issue 2, June 2016.

[J17] A. Psarras, J. Lee, I. Seitanidis, C. Nicopoulos, and G. Dimitrakopoulos, "PhaseNoC: Versatile Network Traffic Isolation Through TDM-Scheduled Virtual Channels," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Volume 35, Issue 5, pp. 844-857, May 2016.

[J16] M.A. Skitsas, C. Nicopoulos, and M.K. Michael, "DaemonGuard: Enabling O/S-Orchestrated Fine-Grained Software-Based Selective-Testing in Multi-/Many-Core Microprocessors," in *IEEE Transactions on Computers (TC)*, Volume 65, Issue 5, pp. 1453-1466, May 2016.

[J15] M. Kleanthous, Y. Sazeides, E. Ozer, C. Nicopoulos, P. Nikolaou, and Z. Hadjilambrou, "Toward Multi-Layer Holistic Evaluation of System Designs," in *IEEE Computer Architecture Letters (CAL)*, Volume 15, Issue 1, January–June 2016.

[J14] I. Seitanidis, A. Psarras, K. Chrysanthou, C. Nicopoulos, and G. Dimitrakopoulos, "ElastiStore: Flexible Elastic Buffering for Virtual-Channel-Based Networks on Chip," in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 23, Issue 12, pp. 3015-3028, December 2015.

[J13] S. Kang, C. Nicopoulos, A. Gavriloska, and J. Kim, "Subtleties of Run-Time Virtual Address Stacks," in *IEEE Computer Architecture Letters (CAL)*, Vol. 14, Issue 2, pp. 152-155, July–December 2015.

[J12] S. Baek, H.G. Lee, C. Nicopoulos, J. Lee, and J. Kim, "Size-Aware Cache Management for Compressed Cache Architectures," in *IEEE Transactions on Computers (TC)*, Vol. 64, Issue 8, pp. 2337-2352, August 2015.

[J11] S. Baek, H.G. Lee, C. Nicopoulos, and J. Kim, "Designing Hybrid DRAM/PCM Main Memory Systems Utilizing Dual-Phase Compression," in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 20, Issue 1, Article No. 11, November 2014.

[J10] J. Lee, C. Nicopoulos, H.G. Lee, and J. Kim, "Centaur: a Hybrid Network-on-Chip Architecture Utilizing Micro-Network Fusion," in *Springer Journal of Design Automation for Embedded Systems (DAEM)*, Volume 18, Issue 3, pp. 121-139, September 2014.

[J9] J. Lee, C. Nicopoulos, H.G. Lee, and J. Kim, "TornadoNoC: A Lightweight and Scalable On-Chip Network Architecture for the Many-Core Era," in *ACM Transactions on Architecture and Code Optimization (TACO)*, Vol. 10, Issue 4, Article No. 56, December 2013.

[J8] J. Lee, C. Nicopoulos, H.G. Lee, and J. Kim, "Sharded Router: A Novel On-Chip Router Architecture Employing Bandwidth Sharding and Stealing," in *Elsevier Journal of Parallel Computing (PARCO)*, Vol. 39, Issue 9, pp. 372-388, September 2013.

[J7] A. Vitkovskiy, V. Soteriou, and C. Nicopoulos, "Dynamic fault-tolerant routing algorithm for networks-on-chip based on localised detouring paths," in *IET Computers and Digital Techniques Journal*, Vol. 7, Issue 2, pp. 93-103, March 2013.

[J6] J. Lee, C. Nicopoulos, H.G. Lee, S. Panth, S.K. Lim, and J. Kim, "IsoNet: Hardware-based Job Queue Management for Manycore Architectures," in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 21, Issue 6, pp. 1080-1093, June 2013.

[J5] B. Grot, D. Hardy, P. Lotfi-Kamran, C. Nicopoulos, Y. Sazeides, and B. Falsafi, "Optimizing Datacenter TCO with Scale-Out Processors," in *IEEE Micro*, Vol. 32, Issue 5, September-October 2012.

[J4] A. Vitkovskiy, V. Soteriou, and C. Nicopoulos, "A Dynamically Adjusting Gracefully Degrading Link-Level Fault-Tolerant Mechanism for NoCs," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 31, Issue 8, pp. 1235-1248, August 2012.

[J3] F. Wang, Y. Chen, C.A. Nicopoulos, X. Wu, Y. Xie, and N. Vijaykrishnan, "Variation-aware Task and Communication Mapping for MPSoC Architecture," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 30, Issue 2, pp. 295-307, February 2011.

[J2] C.A. Nicopoulos, S. Srinivasan, A. Yanamandra, D. Park, N. Vijaykrishnan, C.R. Das, and M.J. Irwin, "On the Effects of Process Variation in Network-on-Chip Architectures," in the *IEEE Transactions on Dependable and Secure Computing (TDSC)*, Vol. 7, Issue 3, pp. 240-254, July-September 2010.

[J1] A. Cevrero, P. Athanasopoulos, H.P. Afshar, A.K. Verma, P. Brisk, F.K. Gurkaynak, C.A. Nicopoulos, Y. Leblebici, and P. Ienne, "The Field-Programmable Compressor Tree: a Programmable IP Core for Improved FPGA Arithmetic Performance," in the *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, Vol. 2, Issue 2, Article 13, pp. 13:1-13:36, June 2009.

Conference Proceedings

Note: Top-tier (Flagship) Computer Architecture Conferences

C. Nicopoulos has **7 publications** in the flagship conferences of computer architecture:

- International Symposium on Computer Architecture (**ISCA**)
- International Symposium on Microarchitecture (**MICRO**)
- International Symposium on High Performance Computer Architecture (**HPCA**)

These conferences have very high impact factors, and all three are in the top 10 of **Google Scholar's Top Publications in Computing Systems** (based on number of citations, and including *both* journals and conferences):

`https://scholar.google.com/citations?view_op=top_venues&hl=en&vq=eng_computingsystems`

The 7 aforementioned publications are [**C32,C31,C14,C10,C9,C7,C6**], as shown below. These 7 publications have received numerous citations (**see Google Scholar** for up-to-date statistics).

NB: See *Google Scholar* for detailed and up-to-date citation statistics

[C53] D. Konstantinou, A. Psarras, C. Nicopoulos, and G. Dimitrakopoulos, "Low-Power Dual-Edge-Triggered Synchronous Latency-Insensitive Systems," in *Proceedings of the IEEE International Conference on Modern Circuits and Systems Technologies (MOCAST)*, May 2018.

[C52] J. Lee, M. Debnath, A. Patki, M. Hasan, and C. Nicopoulos, "Hardware-based Online Self-diagnosis for Faulty Device Identification in Large-scale IoT Systems," in *Proceedings of the ACM/IEEE International Conference on Internet-of-Things Design and Implementation (IoTDI)*, April 2018.

[C51] N. Zompakis, M. Noltsis, L. Ndreu, Z. Hadjilambrou, P. Englezakis, P. Nikolaou, A. Portero, S. Libutti, G. Massari, F. Sassi, A. Bacchini, C. Nicopoulos, Y. Sazeides, R. Vavrik, M. Golasowski, J. Sevcik, V. Vondrak, F. Catthoor, W. Fornaciari, and D. Soudris, "HARPA: Tackling Physically Induced Performance Variability," in *Proceedings of the Design Automation and Test in Europe (DATE) Conference*, March 2017.

[C50] M. Debnath, D. Konstatinou, C. Nicopoulos, G. Dimitrakopoulos, W.M. Lin, and J. Lee, "Low-Cost Congestion Management in Networks-on-Chip Using Edge and In-Network Traffic Throttling," in *Proceedings of the International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS)* (held in conjunction with the HiPEAC Conference), January 2017.

[C49] A. Psarras, S. Moisidis, C. Nicopoulos, and G. Dimitrakopoulos, "RapidLink: a Network-on-Chip Architecture with Double-Data-Rate Links," in *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, December 2016.

[C48] I. Seitanidis, C. Nicopoulos, and G. Dimitrakopoulos, "PowerMax: an automated methodology for generating peak-power traffic in networks-on-chip," in *Proceedings of the IEEE Symposium on Networks-on-Chip (NOCS)*, September 2016.

[Best Paper Award Nominee]

[C47] A. Psarras, J. Lee, P.M. Mattheakis, C. Nicopoulos, and G. Dimitrakopoulos, "A Low-Power Network-on-Chip Architecture for Tile-based Chip Multi-Processors," in *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, May 2016.

[C46] M. Paschou, A. Psarras, C. Nicopoulos, and G. Dimitrakopoulos, "CrossOver: Clock Domain Crossing under Virtual-Channel Flow Control," in *Proceedings of Design Automation and Test in Europe (DATE) Conference*, March 2016.

[C45] M. Skitsas, C. Nicopoulos, and M.K. Michael, "Toward efficient check-pointing and rollback under on-demand SBST in chip multi-processors," in *Proceedings of the IEEE International On-Line Testing Symposium (IOLTS)*, July 2015.

[C44] A. Panteloukas, A. Psarras, C. Nicopoulos, and G. Dimitrakopoulos, "Timing-resilient Network-on-Chip architectures," in *Proceedings of the IEEE International On-Line Testing Symposium (IOLTS)*, July 2015.

[C43] D. Rodopoulos, S. Corbetta, G. Massari, S. Libutti, F. Catthoor, Y. Sazeides, C. Nicopoulos, A. Portero, E. Cappe, R. Vavrik, V. Vondrak, D. Soudris, F. Sassi, A. Fritsch, and W. Fornaciari, "HARPA: Solutions for Dependable Performance under Physically Induced Performance Variability," in *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, July 2015.

[C42] D. Rodopoulos, Y. Sazeides, F. Catthoor, C. Nicopoulos, and D. Soudris, "Sensitivity of SRAM Cell Most Probable SNM Failure Point to Time-Dependent Variability," in *Proceedings of the 11th Workshop on Silicon Errors in Logic – System Effects (SELSE)*, March 2015.

[C41] A. Psarras, I. Seitanidis, C. Nicopoulos, and G. Dimitrakopoulos, "PhaseNoC: TDM scheduling at the virtual-channel level for efficient network traffic isolation," in *Proceedings of Design Automation and Test in Europe (DATE) Conference*, March 2015.

[**Best Paper Award – Europe's premiere and biggest electronic system design & test conference** – *Acceptance Rate: 22.4% (for long/short presentations)*]

[C40] M. Skitsas, C. Nicopoulos, and M.K. Michael, "Exploring check-pointing and rollback recovery under selective SBST in Chip Multi- Processors," in *Proceedings of the Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN)*, March 2015.

[C39] M. Skitsas, C. Nicopoulos, and M.K. Michael, "Exploration of System Availability During Software-Based Self-Testing in Many-core Systems under Test Latency Constraints," in *Proceedings of the IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, October 2014.

[C38] I. Seitanidis, A. Psarras, E. Kalligeros, C. Nicopoulos, and G. Dimitrakopoulos, "ElastiNoC: A Self-Testable Distributed VC-based Network-on-Chip Architecture," in *Proceedings of the IEEE Symposium on Networks-on-Chip (NOCS)*, September 2014.

[C37] I. Seitanidis, A. Psarras, G. Dimitrakopoulos, and C. Nicopoulos, "ElastiStore: An elastic buffer architecture for Network-on-Chip routers," in *Proceedings of Design Automation and Test in Europe (DATE) Conference*, March 2014.

[C36] J. Lee, C. Nicopoulos, G.H. Oh, S.W. Lee, and J. Kim, "Hardware-assisted Intrusion Detection by Preserving Reference Information Integrity," in *Proceedings of the 13th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP)*, December 2013.

[C35] M.A. Skitsas, C. Nicopoulos, and M.K. Michael, "DaemonGuard: O/S-assisted selective software-based Self-Testing for multi-core systems," in *Proceedings of the IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, October 2013.

[C34] J. Lee, C. Nicopoulos, S.J. Park, M. Swaminathan, and J. Kim, "Do We Need Wide Flits in Networks-On-Chip?" in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, August 2013.

[C33] G. Dimitrakopoulos, N. Georgiadis, C. Nicopoulos, E. Kalligeros, "Switch Folding: Network-on-Chip Routers with Time-Multiplexed Output Ports," in *Proceedings of the Design, Automation, and Test in Europe (DATE) Conference*, March 2013.

[C32] S. Baek, H.G. Lee, C. Nicopoulos, J. Lee, and J. Kim, "ECM: Effective Capacity Maximizer for High-Performance Compressed Caching," in *Proceedings of the 19th IEEE International Symposium on High Performance Computer Architecture (**HPCA**)*, 12 pages, February 2013.

[**Highly cited** (see Google Scholar) – **Flagship conference in Computer Architecture** – *Acceptance Rate: 20.5%*]

[C31] A. Prodromou, A. Panteli, C. Nicopoulos, and Y. Sazeides, "NoCAlert: An On-Line and Real-Time Fault Detection Mechanism for Network-on-Chip Architectures," in *Proceedings of the 45th Annual International Symposium on Microarchitecture (**MICRO**)*, 12 pages, December 2012.

[**Highly cited** (see Google Scholar) – **HiPEAC 2012 Paper Award – Flagship conference in Computer Architecture** – *Acceptance Rate: 17.5%*]

[C30] D. Milojevic, S. Idgunji, D. Jevdjic, E. Ozer, P. Lotfi-Kamran, A. Panteli, A. Prodromou, C. Nicopoulos, D. Hardy, B. Falsafi, and Y. Sazeides, "Thermal Characterization of Cloud Workloads on a Low-power Server-on-Chip," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, October 2012.

[C29] M. Evripidou, C. Nicopoulos, V. Soteriou, and J. Kim, "Virtualizing Virtual Channels for Increased Network-on-Chip Robustness and Upgradeability," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 21-26, August 2012.

[C28] H.G. Lee, S. Baek, J. Kim, and C. Nicopoulos, "A Compression-based Hybrid MLC/SLC Management Technique for Phase-Change Memory Systems," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 386-391, August 2012.

[C27] M. Skitsas, C. Nicopoulos, and M. Michael, "Toward Selective Software-Based Self-Testing in Future Multi-Core Microprocessors," in *Proceedings of the Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN)*, pp. 71-75, June 2012.

[C26] J. Lee, H.G. Lee, S. Ha, J. Kim, and C. Nicopoulos, "A Programmable Processing Array Architecture Supporting Dynamic Task Scheduling and Module-Level Prefetching," in *Proceedings of the ACM International Conference on Computing Frontiers*, pp. 153-162, May 2012.

[C25] S. Baek, H.G. Lee, C. Nicopoulos, and J. Kim, "A Dual-Phase Compression Mechanism for Hybrid DRAM/PCM Main Memory Architectures," in *Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 345-350, May 2012.

[C24] J. Lee, C. Nicopoulos, H.G. Lee, D. Shin, and J. Kim, "Hermes: Scalable Load Distribution Engine for General-Purpose Computing on Graphics Processing Units (GPGPU)," in *Proceedings of the International Conference on Electronics, Information, and Communication (ICEIC)*, pp. N/A (digital only), February 2012.

[C23] A. Vitkovskiy, V. Soteriou, and C. Nicopoulos, "A Highly Robust Distributed Fault-Tolerant Routing Algorithm for NoCs with Localized Rerouting," in *Proceedings of the Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC)* (held in conjunction with the HiPEAC Conference), pp. 29-32, January 2012.

[C22] H.G. Lee, S. Baek, C. Nicopoulos, and J. Kim, "An energy- and performance-aware DRAM cache architecture for hybrid DRAM/PCM main memory systems," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 381-387, October 2011.

[C21] S. Kang, C. Nicopoulos, H.G. Lee, and J. Kim, "A High-Performance and Energy-Efficient Virtually Tagged Stack Cache Architecture for Multi-core Environments," In *Proceedings of the IEEE International Conference on High Performance Computing and Communications (HPCC)*, pp. 58-67 (10 pages), September 2011.

[**Best Paper Award**]

[C20] J. Lee, C.A. Nicopoulos, Y. Lee, H. Lee, and J. Kim, "Hardware-based Job Queue Management for Manycore Architectures and OpenMP Environments," in *Proceedings of the International Parallel & Distributed Processing Symposium (IPDPS)*, pp. 407-418 (12 pages), May 2011.

[**Best Paper Award Nominee – Architecture Track** – *Acceptance Rate: 19.6%*]

[C19] M. Diao, C.A. Nicopoulos, and J. Kim, "Large-Scale Semantic Concept Detection on Manycore Platforms for Multimedia Mining," in *Proceedings of the International Parallel & Distributed Processing Symposium (IPDPS)*, pp. 384-394 (11 pages), May 2011.

[*Acceptance Rate: 19.6%*]

[C18] A. Vitkovskiy, V. Soteriou, and C.A. Nicopoulos, "A Fine-Grained Link-Level Fault Tolerant Mechanism for NoCs," in *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 447-454, October 2010.

[C17] E. Ozer, K. Flautner, S. Idgunji, A. Saidi, Y. Sazeides, B. Ahsan, N. Ladas, C. Nicopoulos, I. Sideris, B. Falsafi, A. Adileh, M. Ferdman, P. Lotfi-Kamran, M. Kuulusa, P. Marchal, and N. Minas, "EuroCloud: Energy-conscious 3D Server-on-Chip for Green Cloud Services," in *Proceedings of 2nd Workshop on Architectural Concerns in Large Datacenters* (held in conjunction with the ISCA Conference), June 2010.

[C16] S. Hosein, A. Cevrero, P. Brisk, C.A. Nicopoulos, F.K. Gurkaynak, Y. Leblebici, and P. Ienne, "Design Space Exploration for Field Programmable Compressor Trees," in *Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 207-216 (10 pages), 2008.

[C15] N. Soundararajan, A. Yanamandra, C.A. Nicopoulos, N. Vijaykrishnan, A. Sivasubramaniam, and M.J. Irwin, "Analysis and solutions to Issue Queue Process Variation," in *Proceedings of the International Conference on Dependable Systems and Networks (DSN)*, pp. 11-21 (11 pages), 2008.

[C14] R. Das, A.K. Mishra, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, R. Iyer, M.S. Yousif, C.R. Das, "Performance and Power Optimization through Data Compression in Network-on-Chip Architectures," in *Proceedings of the 14th International Symposium on High-Performance Computer Architecture (**HPCA**)*, pp. 215-225 (12 pages), 2008.

[**Highly cited** (see Google Scholar) – **Flagship conference in Computer Architecture** – *Acceptance Rate: 19%*]

[C13] C.A. Nicopoulos, A. Yanamandra, S. Srinivasan, N. Vijaykrishnan, and M.J. Irwin, "Variation-Aware Low-Power Buffer Design," in *Proceedings of the 41st Asilomar Conference on Signals, Systems, and Computers*, pp. 1402-1406, 2007.

[C12] F. Wang, C.A. Nicopoulos, X. Wu, Y. Xie, and N. Vijaykrishnan, "Variation-aware Task Allocation and Scheduling for MPSoC," in *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pp. 598-603, 2007.

[C11] D. Park, R. Das, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, R. Iyer, and C. R. Das, "Design of a Dynamic Priority-Based Fast Path Architecture for On-Chip Interconnects," in *Proceedings of the 15th IEEE Symposium on High-Performance Interconnects (Hot Interconnects)*, pp. 15-20, 2007.

[C10] J. Kim, C.A. Nicopoulos, D. Park, R. Das, Y. Xie, N. Vijaykrishnan, and C.R. Das, "A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures," in *Proceedings of the 34th Annual International Symposium on Computer Architecture (**ISCA**)*, pp. 138-149 (12 pages), 2007.

[**Highly cited** (see Google Scholar) – **Flagship conference in Computer Architecture** – *Acceptance Rate: 22.5%*]

[C9] C.A. Nicopoulos, D. Park, J. Kim, N. Vijaykrishnan, M.S. Yousif, and C.R. Das, "ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers," in *Proceedings of the 39th Annual International Symposium on Microarchitecture (**MICRO**)*, pp. 333-344 (12 pages), 2006.

[**Highly cited** (see Google Scholar) – **Flagship conference in Computer Architecture** – *Acceptance Rate: 24%*]

[C8] D. Park, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, and C.R. Das, "A Distributed Multi-Point Network Interface for Low-Latency, Deadlock-Free On-Chip Interconnects," in *Proceedings (electronic) of the International Conference on Nano-Networks (Nano-Net)*, 2006.

[C7] F. Li, C.A. Nicopoulos, T. Richardson, Y. Xie, N. Vijaykrishnan, and M. Kandemir, "Design and Management of 3D Chip Multiprocessors Using Network-in-Memory," in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (**ISCA**)*, pp. 130-141 (12 pages), 2006.

[**Highly cited** (see Google Scholar) – **Flagship conference in Computer Architecture** – *Acceptance Rate: 13%*]

[C6] J. Kim, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, M.S. Yousif, and C.R. Das, "A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks," in *Proceedings of the 33rd Annual International Symposium on Computer Architecture (**ISCA**)*, pp. 4-15 (12 pages), 2006.

[**Highly cited** (see Google Scholar) – **Flagship conference in Computer Architecture** – *Acceptance Rate: 13%*]

[C5] D. Park, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, and C.R. Das, "Exploring Fault-Tolerant Network-on-Chip Architectures," in *Proceedings of the International Conference on Dependable Systems and Networks (DSN)*, pp. 93-102 (10 pages), 2006.

[**Highly cited** (see Google Scholar)]

[C4] J. Kim, D. Park, C.A. Nicopoulos, N. Vijaykrishnan, and C.R. Das, "Performance Enhancement through Early Release and Buffer Optimization in Network-on-Chip Router Architectures," in *Special Workshop on Future Interconnects and Networks on Chip* at the Design, Automation and Test in Europe (DATE) Conference, 2006.

[C3] T.D. Richardson, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, Yuan Xie, C.R. Das, and V. Degalahal, "A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks," in *Proceedings of the 19th International Conference on VLSI Design*, pp. 657-664, 2006.

[C2] J. Kim, D. Park, C.A. Nicopoulos, N. Vijaykrishnan, and C.R. Das, "Design and analysis of an NoC architecture from performance, reliability and energy perspective," in *Proceedings of the Symposium on Architectures for Networking and Communications Systems (ANCS)*, pp. 173-182, 2005.

[**Highly cited** (see Google Scholar)]

[C1] J. S. Kim, C.A. Nicopoulos, N. Vijaykrishnan, Y. Xie, and E. Lattanzi, "A Probabilistic Model for Soft-Error Rate Estimation in Combinational Logic," in *Proceedings of the International Workshop on Probabilistic Analysis Techniques for Real Time and Embedded Systems (PARTES)*, 2004.

Technical Reports

[TR1] J. Kim, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, and C.R. Das, "A Fine-Grained Modular Architecture for System-on-Chip Networks," *Technical Report, CSE-06-013, Department of Computer Science and Engineering, The Pennsylvania State University, University Park, PA, USA*, 2006.

Theses

[Th2] C.A. Nicopoulos, "Network-on-Chip Architectures: A Holistic Design Exploration," *Ph.D. Thesis* (under N. Vijaykrishnan), Department of Electrical Engineering, The Pennsylvania State University, University Park, PA, 2007.

[Th1] C.A. Nicopoulos, "Smart Antennas for Wireless Communications," *Undergraduate Honors Thesis* (under J.F. Doherty), Department of Electrical Engineering, The Pennsylvania State University, University Park, PA, 2003.

Conference Presentations & Invited Talks

[P14] "A Network-on-Chip Router Architecture with Unified and Dynamic Buffer Management," *Graduate Seminar of the Department of Electrical and Computer Engineering, University of Cyprus*, Nicosia, Cyprus, April 2010.

[P13] "Dynamic Virtual Channel Regulation and Buffering for On-Chip Networks," at the *Interconnects Cluster Meeting of the International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC)*, January 2009, Paphos, Cyprus.

[P12] "Network-on-Chip Architectural Exploration," *Poster Presentation at the International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC)*, January 2009, Paphos, Cyprus.

[P11] "The Effects of Process Variation on Network-on-Chip Architectures," *Guest Lecture at the Xi Computer Architecture Research Group Seminar of the Department of Computer Science, University of Cyprus*, Nicosia, Cyprus, October 2008.

[P10] "Exploring On-Chip Interconnection Network Architectures," *Poster Presentation at the European Design and Automation Association (EDAA) Ph.D. Forum at the DATE Conference*, Munich, Germany, March 2008.

[P9] "The New Face of the On-Chip Interconnect," at the *Interconnects Cluster Meeting of the International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC)*, January 2008, Goteborg, Sweden.

[P8] "ViChaR: A Dynamic Virtual Channel Regulator and Unified Buffer Structure for On-Chip Routers," *Focus Center Research Program (FCRP) e-Connect Seminar* (Given to eminent semiconductor industry sponsors by top US research institutions – very competitive presenter selection process), April 2007.

[P7] "3D + NoC: An Emerging Interconnect Paradigm," at *Intel Corporation*, Hillsboro, Oregon, USA, March 2007.

[P6] "ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers," at the 39^{th} *Annual International Symposium on Microarchitecture (MICRO)*, Orlando, Florida, USA, December 2006.

[P5] "Architectural Exploration in NoC Design," at the *GSRC Annual Symposium*, San Jose, California, USA, September 2006.

[P4] "A Novel Decomposable Router Architecture for On-Chip Networks," *Graduate Seminar of the Department of Electrical and Computer Engineering, University of Cyprus*, Nicosia, Cyprus, September 2006.

[P3] "A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks," at the 33^{rd} *Annual International Symposium on Computer Architecture (ISCA)*, Boston, Massachusetts, USA, June 2006.

[P2] "A 3D Network-on-Chip Simulator," at the *GSRC Quarterly Workshop*, Berkeley, California, USA, March 2006.

[P1] "HS3d: Hot Spot 3d," at the *GSRC Quarterly Workshop*, Berkeley, California, USA, March 2006.

Professional Activities & Service

- **Memberships & Affiliations**
  - IEEE Member (plus IEEE Computer Society), 2008 – Present
  - ACM Member (plus SIGARCH and SIGMICRO Special Interest Groups), 2009 – Present
  - High Performance Embedded Architectures and Compilation, HiPEAC Network of Excellence, Full Member, 2014 – Present
  - High Performance Embedded Architectures and Compilation, HiPEAC Network of Excellence, Affiliate Member, 2009 – 2014
  - IEEE Student Member (plus IEEE Computer Society), 2006 – 2008
  - ACM Student Member (plus SIGARCH and SIGMICRO Special Interest Groups), 2006 – 2008
  - Gigascale Systems Research Center (GSRC) Student Member, (`http://www.gigascale.org/`), 2005 – 2007
- **Professional Certifications**
  - Recipient of the Technology Collaborative (formed after the merger of the Pittsburgh Digital Greenhouse and the Robotics Foundry) **Certificate in System-on-Chip Design**, May 2006.
- **Professional Service**
  - **Organizational & Chair Activities**
    - Conference Organization
      - Organizing Committee Member (Web Chair, A/V Chair, and Local Organizing Committee member) of the IEEE European Test Symposium (ETS), 2017
      - Organizing Committee Member of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2012
    - Session Chair
      - 2017 IEEE European Test Symposium (ETS), Limassol, Cyprus
      - 2012 ACM/IEEE International Symposium on Networks-on-Chip (NOCS), Copenhagen, Denmark
      - 2010 HiPEAC Workshop on Design for Reliability (DFR), Pisa, Italy
  - **Technical Program Committee (TPC) Memberships**
    - IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009 – 2013
    - IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI), 2014 – 2016
    - ACM/EDA/IEEE Design Automation Conference (DAC), 2017
    - IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2018 (External Review Committee)
    - IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC), 2017
    - IEEE Design, Automation & Test in Europe Conference (DATE), 2011 – 2014

- IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2011, 2015
- ACM/IEEE International Symposium on Networks-on-Chip (NOCS), 2012, 2015 – Present
- ACM/IEEE International Workshop on Network-on-Chip Architectures (NoCArc) [held in conjunction with the IEEE/ACM International Symposium on Microarchitecture (MICRO)], 2012 – Present
- International Workshop on Interconnection Network Architecture: On-Chip, Multi-Chip (INA-OCMC) [held in conjunction with the HiPEAC Conference], 2012 – 2015
- International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS) [held in conjunction with the HiPEAC Conference], 2016 – Present
- IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), 2014 – Present
- IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2015 – Present
- IEEE European Test Symposium (ETS), 2017
- IEEE/ACM International Conference on VLSI Design, 2014
- Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP), 2015
- Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN), 2014
- Memory Architecture and Organization Workshop (MeAOW), 2014
- International Conference on Parallel Processing (ICPP), 2013
- IEEE Hellenic Student Branch Congress (HSBC), 2013

– **Manuscript Reviewer**

- Reviewer for the four main IEEE/ACM Computer Architecture Conferences (ISCA, MICRO, HPCA, ASPLOS)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Parallel and Distributed Systems (TPDS)
- IEEE Transactions on VLSI (TVLSI)
- IEEE Transactions on Computer Aided Design (TCAD)
- IEEE Computer Architecture Letters (CAL)
- IEEE Embedded Systems Letters
- IEEE Micro Magazine
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- ACM Transactions on Architecture and Code Optimization (TACO)
- ACM Computing Surveys (CSUR)
- ACM Journal of Emerging Technologies in Computing Systems (JETC)
- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Transactions on Parallel Computing (TOPC)
- Swiss National Science Foundation (SNSF)
- Springer Computers & Electrical Engineering
- Springer Design Automation for Embedded Systems
- Springer Frontiers of Computer Science
- Elsevier Computers & Electrical Engineering
- Elsevier Microprocessors and Microsystems
- Elsevier Integration – The VLSI Journal
- Elsevier Journal of Parallel and Distributed Computing (JPDC)
- Elsevier Parallel Computing (PARCO)
- Journal of Circuits, Systems, and Computers (JCSC)
- Journal of Signal Processing Systems
- Hindawi Journal of Electrical and Computer Engineering
- Hindawi VLSI Design

- Reviewer for numerous IEEE/ACM Conferences:
  - NOCS, DAC, DATE, ICCAD, ISLPED, IPDPS, ICS, PACT, HiPEAC, Computing Frontiers, ISVLSI, VLSI Design, ICA3PP, FPL, SiPS, Nano-Net, ICCCAS, CMP-MSI, ISCAS, MELECON

Departmental Service

- Co-organized the 5th Annual Texnopleysi Contest directed towards high-school and technical-school students in 2010, and the 2009 ECE Department Open Day event.
- Co-organized the 2nd Computer Science and Engineering Summer School, held in collaboration with the Department of Computer Science and sponsored by the IEEE Cyprus Section, 22-23 June 2009.
- Departmental Undergraduate Studies Committee, Member, 2014 – Present
- Departmental Committee of Information Technology & Website, Member, 2014 – Present
- Departmental Committee of Outreach & Publications, Member, 2012 – 2014
- Departmental Committee of Information Technology & Website, President, 2010 – 2012
- Departmental Library Liaison (responsible for all library-related issues), 2009 – 2014
- Proctor of the Department's student team in the IEEEXtreme Programming Competition, 2010 – 2015.
- Grader of written examination papers for departmental IT positions, 2011.
- Co-author of written examinations for departmental IT positions, 2010, 2011.
- Member of Tender Evaluation Committee for departmental research equipment, 2012.
- Member of University Interview Committee for departmental IT positions, 2010.

University Service

- Member of Tender Evaluation Committee for university-wide IT purchases (for an upgrade of the university's computing hardware infrastructure), 2015.
- Senate Library Committee, Member (representing the Faculty of Engineering), 2011 – 2014
- Member of Tender Evaluation Committee for university-wide IT purchases, 2010.
- Director of Tender Evaluation Committee for a computer-related purchase of the Department of Psychology, 2009.

Past Academic & Professional Experience

- *August 2003 – August 2007*
  Graduate Research and Teaching Assistant, Department of Electrical Engineering / Department of Computer Science and Engineering, The Pennsylvania State University, USA
  - Research Experience (Member of the Microsystems Design Laboratory, MDL)
    - Research in High-Performance, Area- and Power-Efficient, and Reliable NoC Architectures
    - Research in Computer Architecture
    - Research in VLSI Digital System Design
    - Research in Multi-Processor Systems-on-Chip (MPSoC) and Chip Multi-Processors (CMP)
  - Teaching Experience
    - Teaching Assistant (for four semesters) of the Communication Networks Course (Senior-Level Undergraduate)

- *August 2001 – August 2003*
  Undergraduate Research Assistant, Department of Electrical Engineering, The Pennsylvania State University, USA
  - SPIRIT (Student Projects Involving Rocket Investigation Techniques) Program at Penn State
    - NASA and private-industry-funded research program to build a rocket to carry out experiments in the mesosphere

- Joined the Experiments Group in August 2001, and designed a circuit used to measure electron content/density in the mesosphere
- Conducted pre-launch experiments at NASA Wallops Island Base, in Virginia, USA, under the guidance and supervision of several NASA engineers
- Rocket was successfully launched on 3 October 2003

– Undergraduate Honors Research
- In partial fulfillment of Undergraduate Honors Thesis
- Research (extensive computer programming and simulations) in smart antennas for wireless communications

• *June 2000 – August 2000*
Application Developer and Network Administrator
– CYTANET Internet Service Provider, Cyprus Telecommunications Authority (CYTA), Nicosia, Cyprus
- Set up and maintained Local and Wide Area Networks
- Set up and maintained UNIX and Windows NT Servers, including special-content servers, such as Streaming Audio/Video and WAP (Wireless Application Protocol) Servers
- Participated in CISCO Systems router installation, configuration and maintenance

• *July 1996 – August 1998*
Military Service
– Reserve Officer in the Armored Division of the Cyprus Army
- Attended a military academy for reserve officers in Athens, Greece, specializing in Main Battle Tanks
- Served 26-month military service as an officer, managing four tanks and sixteen men as Commander of a Tank Platoon
- Currently a reserve officer at the rank of First Lieutenant (Ypolochagos)

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